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## **REMARKS**

Claims 1-23 are currently pending in the subject application and are presently under consideration. Claims 11-16 have been amended to correct dependencies; accordingly no new matter has been introduced, no new search is required, and it is respectfully submitted that the amendments should be entered. Favorable reconsideration of the subject patent application is respectfully requested in view of the amendments and comments herein.

## I. Rejection of Claims 1-8, 10, and 17-23 Under 35 U.S.C. §103(a)

Claims 1-8, 10, and 17-23, are rejected under 35 U.S.C. §103(a), as being unpatentable over Singh et al. (U.S. 6,650,422) (Singh et al. '422) in view of Singh et al. (U.S. 6,561,706) (Singh et al. '706). It is respectfully requested that this rejection be withdrawn for at least the following reasons. The cited references, either alone or in combination, fail to teach or suggest all elements of the subject claims.

To reject claims in an application under §103, an examiner must establish a prima facie case of obviousness. A prima facie case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the Applicant's disclosure. See In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicant's claimed invention relates to a combination of non-lithographic shrink techniques and trim processes for gate formation and line-edge roughness reduction. Independent claims 1, 10, and 17 recite similar limitations. Independent claim 1 recites a system for mitigating line-edge roughness, comprising a non-lithographic shrink component and a trim etch component. Independent claim 10 recites a method for mitigating line-edge roughness, comprising determining whether line-edge roughness exists, employing a non-lithographic shrink technique to mitigate line-edge roughness, and employing a trim etch technique to compensate

for any increase in critical dimensions. Independent 17 recites a means-plus-function system for mitigating line-edge roughness and trimming excess resist to achieve a desired critical dimension.

Singh et al. '402 relates to scatterometry techniques to ascertain asymmetry profile of features and generate a feedback or feedforward process control data associated therewith. Independent claims 1, 11, 20, and 24 recite similar limitations, namely directing a beam of radiation at one side of a feature, detecting a first reflected radiation signature from the one side of the feature, directing a beam of radiation at a second side of a feature, detecting a second reflected radiation signature from the second side of the feature, and comparing the first and second detected radiation signatures to determine the asymmetry of the feature. However, Singh et al. '402 is silent with respect to non-lithographic shrink techniques and trim process for gate formation and line-edge roughness reduction. Therefore Singh et al. '402 does not teach or suggest all claim limitations.

The Examiner contends that the difference between the subject claims and Singh et al. '402 is that Singh et al. '402 does not disclose that the pattern profiles determined on the photoresist features are that of line-edge roughness and critical dimensions.

The Examiner utilizes Singh et al. '706 to overcome the deficiencies of Singh et al. '402. Singh et al. '706, in col. 2, lines 14-66, discloses a system that monitors photoresist pattern features and generates information from scatterometric analysis, and controls subsequent processes based on the collected data from monitoring previous processes, and therefore facilitate achieving desired critical dimensions and pattern edge dimensions (uniformity in pattern width and line edge roughness). The Examiner asserts that it would be obvious to a skilled artisan to modify Singh et al. 402by employing the method of monitoring features such as critical dimensions and line-edge roughness as suggested by Singh et al. '706. Applicants' representative respectfully disagrees for at least the following reason. One skilled in the art would not have been motivated to combine Singh et al. '402 and Singh et al. '706 to address the problem of line-edge roughness because Singh et al. '706 does not address line-edge roughness.

Singh et al. '706 relates to critical dimension monitoring from a latent image. Independent claims 1, 8 and 10 recite similar limitations, namely directing light onto a wafer, detecting the light reflected from a wafer, generating a signature from the reflected light and controlling both an exposure process (feedback) and post exposure development and baking

processes (feedforward) based on the signature. However, Singh et al. '706 is silent with respect to mitigating line-edge roughness.

Though the Examiner cites Singh et al. '706, col. 2, lines 14-66 as support for contending that Singh et al. '706 "discloses a system . . . [facilitating] achieving desired critical dimensions and pattern edge dimensions (uniformity in pattern width, and line-edge roughness)." It appears that the Examiner incorrectly equates critical dimensions with uniformity in pattern width, and pattern edge dimensions with line-edge roughness. In the cited passage, Singh et al. '706 only a system for achieving desired critical dimensions is disclosed. See col. 2, lines 30-39. Neither of the terms pattern edge dimensions nor line-edge roughness can be found in the cited passage (col. 2, lines 14-66), nor anywhere in Singh et al. '706.

Problems concerning critical dimensions are not equivalent to problems concerning pattern edge dimensions or *line-edge roughness*. Critical dimensions are the dimensions of the smallest geometrical features (width of interconnect line, contacts, trenches, *etc.*) which can be formed during semiconductor device/circuit manufacturing using given technology. Thus, critical dimensions refer only to spaces between features in the pattern, *not* to the features in the pattern themselves.

Line-edge roughness refers to variations on sidewalls of features. See specification, p. 2, ll. 20-29. Variations on sidewalls of features occur in three dimensions: in the two dimensions that define the vertical plane of the sidewalls of the features, and in a third dimension orthogonal to that vertical plane. Critical dimensions, on the other hand, are relevant in only one dimension: the third dimension orthogonal to the vertical plane described above (i.e., the separation between features).

It is true that variations in the pattern edge dimensions can increase critical dimensions beyond the customer's specification. However, as explained above, *line-edge roughness* (i.e., a three-dimensional problem) is a different problem from critical dimensions (i.e., a one-dimensional problem), and accordingly, is not suggested by either Singh *et al.* '402 or Singh *et al.* '706. It is possible for a pattern to satisfy the critical dimensions of the customer's specification, and yet still exhibit unacceptable *line-edge roughness* in the patterned photoresist.

There is no suggestion or motivation in either Singh et al. '402 or Singh et al. '706 to address the problem of line-edge roughness. Accordingly, the claimed invention is not obvious over these references, and this rejection should be withdrawn.

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## II. Rejection of Claims 9, 11-16 Under 35 U.S.C. §103(a)

Claims 9, 11-16, are rejected under 35 U.S.C. §103(a), as being unpatentable over Singh et al. '402 in view of Singh et al. '706. It is respectfully requested that this rejection be withdrawn for at least the following reasons. Claim 9 depends from independent claim 1, which is allowable subject matter. Similarly, claims 11-16 depend from independent claim 10, which is allowable subject matter. Thus, it is respectfully submitted that this rejection be withdrawn.

## **CONCLUSION**

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063[AMDP981US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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